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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,810	02/23/2004	Hiroyuki Tomimatsu	114371.01	5451
25944	7590	07/26/2005	EXAMINER	
OLIFF & BERRIDGE, PLC			PHAM, HOAI V	
P.O. BOX 19928			ART UNIT	PAPER NUMBER
ALEXANDRIA, VA 22320			2814	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/782,810

Applicant(s)

TOMIMATSU, HIROYUKI

Examiner

Hoai v. Pham

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) 14-23 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☐ Certified copies of the priority documents have been received.
 - 2) ☒ Certified copies of the priority documents have been received in Application No. 10/327968.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2/23/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-13 in the reply filed on June 13, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 8 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8, lines 2-3, "the plurality of the second pads including a group of pads that are electrically connected to **one another** by a wiring" renders the claim indefinite. It is not clear which pads is connected with --second pad with second pad or second pad with first pad--.

Line 6, "the second wire being bonded to **another of the group of pads**" renders the claim indefinite. It is not clear which pads is "**another of the group of pads**".

Claim 12, "a circuit substrate" renders the claim indefinite. The scope of the claim can not be defined. What "a circuit substrate" means?

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

6. Claims 1-5, 7, 9-10, 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Mess et al. [U.S. Pat. 6,900,528].

With respect to claim 1, Mess et al. (figs. 12A and 13, cols. 6-9) discloses a semiconductor device, comprising:

a die pad (70) (see col. 9, lines 45-48);

a plurality of semiconductor chips stacked on one surface of the die pad;

a lead (102A, 102b) extending toward the die pad (see fig. 12A);

a first wire (62) that is bonded to a first pad (54A) of a first semiconductor chip (60A) among the plurality of semiconductor chips and to a second pad (54B) of a second semiconductor chip (60B) among the plurality of semiconductor chips;

a second wire (62) that is bonded to the lead and to one of the first pad and the second pad (see fig. 13); and

a sealing material (84) that seals the plurality of semiconductor chips (see fig. 13).

With respect to claim 2, Mess et al. discloses that the second semiconductor chip (60B) being mounted on the first semiconductor chip (60A), and the second wire (62) being bonded to the lead and to the second pad (see fig. 13).

With respect to claim 3, Mess et al. discloses that the second wire (62) being lead out to pass above the first wire (see fig. 13).

With respect to claim 4, Mess et al. discloses that the second wire (62) being lead out to traverse the first wire (see fig. 13).

With respect to claim 5, Mess et al. discloses that the second wire (62) being overlapped with and bond to the first wire on the second pad (54B) (see fig. 13).

With respect to claim 7, Mess et al. discloses that the second wire (62) being bonded to the second pad (54B) that is bonded to the first wire, while avoiding a bonded section of the first wire (see fig. 13).

With respect to claim 9, Mess et al. discloses that the second pad (54B) being provided with a bump, and the first wire and the second wire being bonded to the second pad through the bump (see fig. 13).

With respect to claim 10, Mess et al. discloses that the second semiconductor chip (60B) being mounted on the first semiconductor chip (60A), and the second wire (62) being bonded to the lead (70) and to the first pad (54A) (see fig. 13).

With respect to claim 12, Mess et al. discloses a circuit, comprising: the semiconductor device according to claim 1 (see fig. 13).

With respect to claim 13, Mess et al. discloses an electronic device, comprising: the semiconductor device according to claim 1 (see fig. 13).

Claims 1, 6, and 10-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Verma et al. [U.S. Pat. 6,731,011].

With respect to claim 1, Verma et al. (fig. 8, cols. 12-14) discloses a semiconductor device, comprising:

- a die pad (72a);

- a plurality of semiconductor chips stacked on one surface of the die pad;

- a lead (72b) extending toward the die pad;

a first wire (68) that is bonded to a first pad (42b) of a first semiconductor chip (40b) among the plurality of semiconductor chips and to a second pad (42a) of a second semiconductor chip (40a) among the plurality of semiconductor chips;

a second wire that is bonded to the lead (72b) and to the first pad (42b); and

a sealing material (88) that seals the plurality of semiconductor chips (see fig. 8).

With respect to claim 6, Verma et al. discloses that the second wire including a ball formed on a tip thereof, and the ball being press-bonded to the first wire (see fig. 8).

With respect to claim 10, Verma et al. discloses that the second semiconductor chip (40a) being mounted on the first semiconductor chip (40b), and the second wire being bonded to the lead (72b) and to the first pad (42b) (see fig. 8).

With respect to claim 11, Verma et al. discloses that the first semiconductor chip (40b) being a memory, and the second semiconductor chip (40a) being a microprocessor (see col. 9, lines 35-50).

With respect to claim 12, Verma et al. discloses a circuit, comprising: the semiconductor device according to claim 1 (see fig. 8).

With respect to claim 13, Verma et al. discloses an electronic device, comprising: the semiconductor device according to claim 1 (see fig. 8).

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-13 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of U.S. Patent No. 6,727,574. Although the conflicting claims are not identical, they are not patentably distinct from each other because the present application merely broadens the claims of U.S. Patent No. 6,727,574.


Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



HOAI V. PHAM
PRIMARY EXAMINER